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	DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ		
☐	L13	l11 and (repair$3 or restor$3)	0
☐	L12	L11 and cache miss	1
☐	L11	predicted load	105
☐	L10	mispredict$4 with load	4
	DB=PGPB,USPT; PLUR=NO; OP=ADJ		
☐	L9	L5 same (repair$3 or restor$3)	15
☐	L8	L6 not l2	4
☐	L7	L6 not l4	4
☐	L6	l5 same (cache miss)	4
☐	L5	mispredict$4 with load	354
☐	L4	L3 same (cache miss)	3
☐	L3	predicted load	186
☐	L2	cache same (load$3 with mispredict$3) same (repair$3 or restor$3)	4
☐	L1	cache same load$3 same mispredict$3 same (repair$3 or restor$3)	153

END OF SEARCH HISTORY

Address-free memory access based on program syntax correlation of loads and stores

Lu Peng Jih-Kwon Peir Qianrong Ma Lai, K.
Dept. of Comput. & Inf. Sci. & Eng., Univ. of Florida, Gainesville, FL, USA
This paper appears in: **Very Large Scale Integration (VLSI) Systems, IEEE Transactions on**

Publication Date: June 2003
On page(s): 314 - 324
Volume: 11 , Issue: 3
ISSN: 1063-8210
Inspec Accession Number: 7720125

Abstract:
An increasing cache latency in next-generation processors incurs profound performance impacts in spite of advanced out-of-order execution techniques. One way to circumvent this cache latency problem is to **predict load values** at the onset of pipeline execution by exploiting either the load value locality or the address correlation of stores and loads. In this paper, we describe a new load value speculation mechanism based on the program syntax correlation of stores and loads. We establish a symbolic cache (SC) , which is accessed in early pipeline stages to achieve a zero-cycle load. Instead of using memory addresses, the SC is accessed by the encoding bits of base register ID plus the displacement directly from the instruction code. Performance evaluations using SPEC95 and SPEC2000 integer programs on SimpleScalar simulation tools show that the SC achieves higher prediction accuracy in comparison with other load value speculation methods, especially when hardware resources are limited.

Index Terms:
cache storage integer programming microprocessor chips pipeline processing storage allocation SPEC2000 SPEC95 SimpleScalar simulation address-free memory access base register ID cache latency displacement value instruction code integer programming load value speculation load-store correlation microprocessor out-of-order pipeline execution program syntax correlation symbolic cache zero-cycle load

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[Abstract] [PDF Full-Text (120KB)]

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[Abstract] [PDF Full-Text (964KB)]

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[Abstract] [PDF Full-Text (128KB)]

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[Abstract] [PDF Full-Text (652KB)]

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[Abstract] [PDF Full-Text (240KB)]

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[Abstract] [PDF Full-Text (1363KB)]

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[Buy Via Ask*IEEE]

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[Abstract] [PDF Full-Text (172KB)]

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[Abstract] [PDF Full-Text (648KB)]

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[Abstract] [PDF Full-Text (1020KB)]

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281-290.
[Abstract] [PDF Full-Text (1056KB)]

Your search matched **3** of **1094442** documents.
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predicted load value Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **A multi-step hourly load forecasting system using neural nets**
Zebulum, R.S.; Vellasco, M.; Pacheco, M.A.; Guedes, K.;
Circuits and Systems, 1995., Proceedings., Proceedings of the 38th Midwest Symposium on , Volume: 1 , 13-16 Aug. 1995
Pages:461 - 464 vol.1

[Abstract] [PDF Full-Text (316 KB)] **IEEE CNF**

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2 **Address-free memory access based on program syntax correlation of loads and stores**
Lu Peng; Jih-Kwon Peir; Qianrong Ma; Lai, K.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 11 , Issue: 3 , June 2003
Pages:314 - 324

[Abstract] [PDF Full-Text (722 KB)] **IEEE JNL**

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3 **A short-term load prediction algorithm for dynamic economic dispatch**
Erkmen, I.; Adanir, T.;
Electrotechnical Conference, 1994. Proceedings., 7th Mediterranean , 12-14 April 1994
Pages:885 - 888 vol.3

[Abstract] [PDF Full-Text (308 KB)] **IEEE CNF**

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☐	L4	(4875160| 5341482| 5440703| 5481693| 5606696| 5717946| 5721867| 5794063| 6055625| 6070238| 6128722)![pn]	11
☐	L3	6442675.pn.	1
☐	L2	6442675.uref.	0
☐	L1	(international business).as. and stream$3 and treat.xa,xp.	52

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L4: Entry 3 of 3 File: PGPB Jul 11, 2002

PGPUB-DOCUMENT-NUMBER: 20020091915
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020091915 A1

TITLE: Load prediction and thread identification in a multithreaded microprocessor

PUBLICATION-DATE: July 11, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Parady, Bodo K.	Danville	CA	US	

APPL-NO: 10/ 044487 [PALM]
DATE FILED: January 11, 2002

RELATED-US-APPL-DATA:
Application is a non-provisional-of-provisional application 60/261435, filed January 11, 2001,

INT-CL: [07] G06 F 9/00, G06 F 12/00

US-CL-PUBLISHED: 712/225; 711/137, 711/213
US-CL-CURRENT: 712/225; 711/137, 711/213

REPRESENTATIVE-FIGURES: 5

ABSTRACT:

A method and apparatus for predicting load addresses and identifying new threads of instructions for execution in a multithreaded processor. A load prediction unit scans an instruction window for load instructions. A load prediction table is searched for an entry corresponding to a detected load instruction. If an entry is found in the table, a load address prediction is made for the load instruction and conveyed to the data cache. If the load addresses misses in the cache, the data is prefetched. Subsequently, if it is determined that the load prediction was incorrect, a miss counter in the corresponding entry in the load prediction table is incremented. If on a subsequent detection of the load instruction, the miss counter has reached a threshold, the load instruction is predicted to miss. In response to the predicted miss, a new thread of instructions is identified for execution.

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of priority to Provisional Application Serial No. 60/261,435 filed Jan. 11, 2001, entitled "Load Prediction and Thread Identification in a Multithreaded Microprocessor."

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L4: Entry 3 of 3 File: PGPB Jul 11, 2002

PGPUB-DOCUMENT-NUMBER: 20020091915
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US-CL-PUBLISHED: 712/225; 711/137, 711/213
US-CL-CURRENT: 712/225; 711/137, 711/213

REPRESENTATIVE-FIGURES: 5

Full - [FULL]
Title - [TI]
Citation - [CIT]
Front - [FRO]
Review - [REV]
Classification - [CLS]
Date - [DATE]
Reference - [REF]
Sequences - [SEQ]
Attachments - [ATT]
Claims - [CLM]
KWIC - [KWIC]
Drwg Desc - [DRAW]
Image - [IMG]

ABSTRACT:

A method and apparatus for predicting load addresses and identifying new threads of instructions for execution in a multithreaded processor. A load prediction unit scans an instruction window for load instructions. A load prediction table is searched for an entry corresponding to a detected load instruction. If an entry is found in the table, a load address prediction is made for the load instruction and conveyed to the data cache. If the load addresses misses in the cache, the data is prefetched. Subsequently, if it is determined that the load prediction was incorrect, a miss counter in the corresponding entry in the load prediction table is incremented. If on a subsequent detection of the load instruction, the miss counter has reached a threshold, the load instruction is predicted to miss. In response to the predicted miss, a new thread of instructions is identified for execution.

CROSS REFERENCE TO RELATED APPLICATIONS

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L4: Entry 3 of 3 File: PGPB Jul 11, 2002

DOCUMENT-IDENTIFIER: US 20020091915 A1
TITLE: Load prediction and thread identification in a multithreaded microprocessor

Detail Description Paragraph:
[0059] FIG. 5 is a flowchart illustrating one embodiment of the load prediction and thread creation mechanism. In block 502, instruction window or buffer is scanned for load instructions. If a load is detected (decision block 504), flow continues to decision block 506. If no load is detected in block 504, control remains with block 502. In decision block 506, a load prediction table is searched for an entry which corresponds to the detected load instruction. If no entry is found for the detected load instruction, execution continues without a prediction, blocks 508 and 510. Subsequent to executing the unpredicted load, an entry is created (block 512) for the load in the load prediction table. On the other hand, if an entry for the detected load is found in the load prediction table (block 506), the effective address of the load is calculated (block 518) and a miss count indicator in the table is checked (block 520) to determine if a load miss is predicted. If a load miss is indicated (block 520), a determination is made as to whether a thread slot is available (block 524). If no thread slot is available, an additional thread is no setup. On the other hand, if a thread slot is available, the load prediction unit scans for the first instruction of a new thread (block 530). In one embodiment, when the first instruction of a new thread is found (block 530), information regarding the new thread is conveyed to the dispatch unit. Such information may include the address of the first instruction of the new thread and a thread unit identifier. Also, subsequent to computing the effective address (block 518) of a detected load, the predicted load is issued (block 522) and executed (block 526). If the predicted load subsequently hits in the data cache (block 534), an indication of this fact along with related information is conveyed to the load prediction unit where the corresponding load prediction table entry is updated (block 538). In one embodiment, this table entry update includes entering the difference between the previous effective address and the current effective address in a stride field of the corresponding entry. In addition, the update includes entering the actual effective address in the table entry. On the other hand, if a cache miss occurs (block 534) a fetch of the data is required (block 536) and an indication of this miss is conveyed to the load prediction unit. The corresponding load prediction table entry is then updated as before (block 538), with the addition of incrementing a miss counter (block 540).

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L4: Entry 2 of 3 File: PGPB Jun 12, 2003

PGPUB-DOCUMENT-NUMBER: 20030110366
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030110366 A1

TITLE: Run-ahead program execution with value prediction

PUBLICATION-DATE: June 12, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wu, Youfeng	Palo Alto	CA	US	
Ngai, Tin-Fook	Santa Clara	CA	US	

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	COUNTRY	TYPE CODE
Intel Corporation				02

APPL-NO: 10/ 017793 [PALM]
DATE FILED: December 12, 2001

INT-CL: [07] G06 F 9/00

US-CL-PUBLISHED: 712/225; 712/239
US-CL-CURRENT: 712/225; 712/239

REPRESENTATIVE-FIGURES: 2

ABSTRACT:

A data processing apparatus, a computer, an article including a machine-accessible medium, and a method of processing data are disclosed. The data processing apparatus may include a pair of pipelines sharing an instruction cache, data cache, and a branch predictor with the second pipeline running ahead of the first pipeline using a data value prediction module. The pipelines may be included in one or more processors and coupled to a memory to form a computer. The method includes executing a plurality of instructions using the pipeline pair, such that when a cache miss is encountered by the second pipeline during execution of a LOAD instruction, the data value prediction module supplies a predicted load value in lieu of a cached value, enabling continued execution of the plurality of instructions by the second pipeline without waiting for the return of the cached value.

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predicted load value<and>(recover or repair) Search

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1 **Hybrid load-value predictors**
Burtscher, M.; Zorn, B.G.;
Computers, IEEE Transactions on , Volume: 51 , Issue: 7 , July 2002
Pages:759 - 774

[Abstract] [PDF Full-Text (2294 KB)] **IEEE JNL**

2 **Active virtual network management prediction: complexity as a framework for prediction, optimization, and assurance**
Bush, S.F.;
DARPA Active NEtworks Conference and Exposition, 2002. Proceedings , 29-30 May 2002
Pages:534 - 553

[Abstract] [PDF Full-Text (710 KB)] **IEEE CNF**

Full-text Search Prototype Results

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16 **Improving value communication for thread-level speculation**
Steffan, J.G.; Colohan, C.B.; Zhai, A.; Mowry, T.C.;
High-Performance Computer Architecture, 2002. Proceedings. Eighth International Symposium on , 2-6 Feb. 2002
Pages:65 - 75

[Abstract] [PDF Full-Text (441 KB)] **IEEE CNF**

17 **Rule-based determination of plant operating state to avoid governor valve instabilities on a 500 MW turbogenerator**
Neal, P.W.; Waddington, J.;
Exploiting the Knowledge Base: Applications of Rule Based Control, IEE Colloquium on , 1 Jun 1989
Pages:5/1 - 5/4

[Abstract] [PDF Full-Text (196 KB)] **IEE CNF**

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load prediction<and>(recover or repair) Search

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1 **Hybrid load-value predictors**
Burtscher, M.; Zorn, B.G.;
Computers, IEEE Transactions on , Volume: 51 , Issue: 7 , July 2002
Pages:759 - 774

[Abstract] [PDF Full-Text (2294 KB)] IEEE JNL

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2 **Influence of temperature and load forecast uncertainty on estimates of power generation production costs**
Valenzuela, J.; Mazumdar, M.; Kapoor, A.;
Power Systems, IEEE Transactions on , Volume: 15 , Issue: 2 , May 2000
Pages:668 - 674

[Abstract] [PDF Full-Text (128 KB)] IEEE JNL

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3 **A feedback linearizing control scheme for a PWM converter-inverter having a very small DC-link capacitor**
Jinhwan Jung; Sunkyoung Lim; Kwanghee Nam;
Industry Applications, IEEE Transactions on , Volume: 35 , Issue: 5 , Sept.-Oct. 1999
Pages:1124 - 1131

[Abstract] [PDF Full-Text (532 KB)] IEEE JNL

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4 **Operation and management of the electric system for industrial plants: an expert system prototype for load-shedding operator assistance**
Croce, F.; Delfino, B.; Fazzini, P.A.; Massucco, S.; Morini, A.; Silvestro, F.; Sivieri,

M.;
Industry Applications, IEEE Transactions on , Volume: 37 , Issue: 3 , May-June 2001
Pages:701 - 708

[Abstract] [PDF Full-Text (192 KB)] IEEE JNL

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5 **Load recovery in the pulp and paper industry following a disturbance**
Agneholm, E.; Daalder, J.E.;
Power Systems, IEEE Transactions on , Volume: 15 , Issue: 2 , May 2000
Pages:831 - 837

[Abstract] [PDF Full-Text (116 KB)] IEEE JNL

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6 **Forecasting power market clearing price and its discrete PDF using a Bayesian-based classification method**
Ni, E.; Luh, P.B.;
Power Engineering Society Winter Meeting, 2001. IEEE , Volume: 3 , 28 Jan.-1 Feb. 2001
Pages:1518 - 1523 vol.3

[Abstract] [PDF Full-Text (636 KB)] IEEE CNF

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7 **Active virtual network management prediction: complexity as a framework for prediction, optimization, and assurance**
Bush, S.F.;
DARPA Active NEtworks Conference and Exposition, 2002. Proceedings , 29-30 May 2002
Pages:534 - 553

[Abstract] [PDF Full-Text (710 KB)] IEEE CNF

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8 **Optimal integrated generation bidding and scheduling with risk management under a deregulated daily power market**
Ni, E.; Luh, P.B.;
Power Engineering Society Winter Meeting, 2002. IEEE , Volume: 1 , 27-31 Jan. 2002
Pages:70 - 76 vol.1

[Abstract] [PDF Full-Text (121 KB)] IEEE CNF

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9 **IEEE Guide For Transmission Structure Foundation Design And Testing**

IEEE Std 691-2001 , 2001
Pages:0_1 - 186

[Abstract] [PDF Full-Text (107494 KB)] IEEE STD

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load prediction<and>(cache miss) Search

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1 **DCache warn:an I-fetch policy to increase SMT efficiency**
Cazorla, F.J.; Ramirez, A.; Valero, M.; Fernandez, E.;
Parallel and Distributed Processing Symposium, 2004. Proceedings. 18th International , April 26-30, 2004
Pages:74 - 83

[Abstract] [PDF Full-Text (1506 KB)] **IEEE CNF**

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2 **Efficient and adaptive Web replication using content clustering**
Yan Chen; Lili Qiu; Weiyu Chen; Luan Nguyen; Katz, R.H.;
Selected Areas in Communications, IEEE Journal on , Volume: 21 , Issue: 6 , Aug. 2003
Pages:979 - 994

[Abstract] [PDF Full-Text (1232 KB)] **IEEE JNL**

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3 **A decoupled predictor-directed stream prefetching architecture**
Sair, S.; Sherwood, T.; Calder, B.;
Computers, IEEE Transactions on , Volume: 52 , Issue: 3 , March 2003
Pages:260 - 276

[Abstract] [PDF Full-Text (1356 KB)] **IEEE JNL**

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4 **Hybrid load-value predictors**
Burtscher, M.; Zorn, B.G.;
Computers, IEEE Transactions on , Volume: 51 , Issue: 7 , July 2002
Pages:759 - 774

[Abstract] [PDF Full-Text (2294 KB)] IEEE JNL

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JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Book reviews - Satellite communications**
Dundas, P.;
Communications Magazine, IEEE , Volume: 22 , Issue: 11 , Nov 1984
Pages:67 - 67

[Abstract] [PDF Full-Text (152 KB)] IEEE JNL

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2 **Productivity measurement in the service sector-a new approach necessity**
Batista, G.B.; Dunda, M.F.E.; Filho, C.S.;
Management of Engineering and Technology, 1999. Technology and Innovation Management. PICMET '99. Portland International Conference on , Volume: 1 , 25-29 July 1999
Pages:394 vol.1

[Abstract] [PDF Full-Text (52 KB)] IEEE CNF

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3 **Comparative investigation of plating conditions on self-annealing of electrochemically deposited copper films**
Ritzdorf, T.; Chen, L.; Fulton, D.; Dundas, C.;
Interconnect Technology, 1999. IEEE International Conference , 24-26 May 1999
Pages:287 - 289

[Abstract] [PDF Full-Text (244 KB)] IEEE CNF

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4 **The measurement of sea-surface temperature in the presence of aerosol contamination with the Along Track Scanning Radiometer (ATSR)**
Dundas, R.M.;
OCEANS '94. 'Oceans Engineering for Today's Technology and Tomorrow's Preservation.' Proceedings , Volume: 1 , 13-16 Sept. 1994

Pages:I/791 - I/794 vol.1

[Abstract] [PDF Full-Text (640 KB)] IEEE CNF

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Quick Tips

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  ```
  sales offices
  ```

  You can also enter a full question or concept in plain language.

  ```
  Where are the sales offices?
  ```

- Capitalize proper nouns to search for specific people, places, or products.

  ```
  John Colter, Netscape Navigator
  ```

- Enclose a phrase in double quotes to search for that exact phrase.

  ```
  "museum of natural history" "museum of modern art"
  ```

- Narrow your searches by using a + if a search term must appear on a page.

  ```
  museum +art
  ```

- Exclude pages by using a - if a search term must not appear on a page.

  ```
  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Nothing Found

Your search for **+abstract:(predicted +abstract:load +abstract:value) +abstract:restore** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

Quick Tips

- Enter your search terms in lower case with a space between the terms.

```
sales offices
```

  You can also enter a full question or concept in plain language.

```
Where are the sales offices?
```

- Capitalize proper nouns to search for specific people, places, or products.

```
John Colter, Netscape Navigator
```

- Enclose a phrase in double quotes to search for that exact phrase.

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Nothing Found

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museum +"natural history" dinosaur -Chicago
```

Nothing Found

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Please review the Quick Tips below or for more information see the Search Tips.

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  John Colter, Netscape Navigator
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  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Nothing Found

Your search for **+abstract:predict +abstract:load +abstract:recover** did not return any results.

You may want to try an Advanced Search for additional options.

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Quick Tips

- Enter your search terms in lower case with a space between the terms.

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Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
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Nothing Found

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Nothing Found

Your search for **+title:predict +title:load +title:repair** did not return any results.

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Terms used **predicted load value** Found **7** of **145,831**

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Relevance scale

1 Static load classification for improving the value predictability of data-cache misses

Martin Burtscher, Amer Diwan, Matthias Hauswirth

May 2002 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2002 Conference on Programming language design and implementation**, Volume 37 Issue 5

Full text available: pdf(273.26 KB) Additional Information: full citation, abstract, references, index terms

While caches are effective at avoiding most main-memory accesses, the few remaining memory references are still expensive. Even one cache miss per one hundred accesses can double a program's execution time. To better tolerate the data-cache miss latency, architects have proposed various speculation mechanisms, including load-value prediction. A load-value predictor guesses the result of a load so that the dependent instructions can immediately proceed without having to wait for the memory access ...

Keywords: load-value prediction, type-based analysis

2 On the value locality of store instructions

Kevin M. Lepak, Mikko H. Lipasti

May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(149.50 KB) Additional Information: full citation, abstract, references, citings, index terms

Value locality, a recently discovered program attribute that describes the likelihood of the recurrence of previously-seen program values, has been studied enthusiastically in the recent published literature. Much of the energy has focused on refining the initial efforts at predicting load instruction outcomes, with the balance of the effort examining the value locality of either all register-writing instructions, or a focused subset of them. Surprisingly, there has been very little publish ...

3 Access region locality for high-bandwidth processor memory system design

Sangyeun Cho, Pen-Chung Yew, Gyungho Lee

November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.43 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper studies an interesting yet less explored behavior of memory access instructions, called access region locality. Unlike the traditional temporal and spatial data locality that

focuses on individual memory locations and how accesses to the locations are inter-related, the access region locality concerns with each static memory instruction and its range of access locations at run time. We consider program's data, heap, and stack regions in this paper. Our experimental study ...

4 Storageless value prediction using prior register values
Dean M. Tullsen, John S. Seng
May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2
Full text available: pdf(116.45 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents a technique called register value prediction (RVP) which uses a type of locality called register-value reuse. By predicting that an instruction will produce the value that is already stored in the destination register, we eliminate the need for large value buffers to enable value prediction. Even without the large buffers, register-value prediction can be made as or more effective than last-value prediction, particularly with the aid of compiler management of values in the re ...

5 The predictability of data values
Yiannakis Sazeides, James E. Smith
December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.28 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

The predictability of data values is studied at a fundamental level. Two basic predictor models are defined: Computational predictors perform an operation on previous values to yield predicted next values. Examples we study are stride value prediction (which adds a delta to a previous value) and last value prediction (which performs the trivial identity operation on the previous value); Context Based} predictors match recent value history (context) with previous value history and predict values ...

Keywords: Prediction, Value Prediction, Context Based Prediction, Stride Prediction, Last Value Prediction

6 Value locality and load value prediction
Mikko H. Lipasti, Christopher B. Wilkerson, John Paul Shen
September 1996 **Proceedings of the seventh international conference on Architectural support for programming languages and operating systems**, Volume 31 , 30 Issue 9 , 5
Full text available: pdf(1.36 MB) Additional Information: full citation, abstract, references, citings, index terms

Since the introduction of virtual memory demand-paging and cache memories, computer systems have been exploiting spatial and temporal locality to reduce the average latency of a memory reference. In this paper, we introduce the notion of *value locality,* a third facet of locality that is frequently present in real-world programs, and describe how to effectively capture and exploit it in order to perform *load value prediction.* Temporal and spatial locality are attributes of storage l ...

7 Microarchitectures: Scaling the issue window with look-ahead latency prediction
Yongxiang Liu, Anahita Shayesteh, Gokhan Memik, Glenn Reinman
June 2004 **Proceedings of the 18th annual international conference on Supercomputing**
Full text available: pdf(302.66 KB) Additional Information: full citation, abstract, references, index terms

In contemporary out-of-order superscalar design, high IPC is mainly achieved by exposing high instruction level parallelism (ILP). Scaling issue window size can certainly provide more ILP; however, future processor scaling demands threaten to limit the size of the issue window.In this study, we propose a dynamic instruction sorting mechanism that provides more ILP without increasing the size of the issue window. In our approach, early in the pipeline, we predict how long an instruction needs to ...

Keywords: CLP, LHT, MNM, SILO, instruction sorting

Results 1 - 7 of 7

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☐	L3	predicted load	186
☐	L2	cache same (load$3 with mispredict$3) same (repair$3 or restor$3)	4
☐	L1	cache same load$3 same mispredict$3 same (repair$3 or restor$3)	153

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☐	L8	L6 not l2	4
☐	L7	L6 not l4	4
☐	L6	l5 same (cache miss)	4
☐	L5	mispredict$4 with load	354
☐	L4	L3 same (cache miss)	3
☐	L3	predicted load	186
☐	L2	cache same (load$3 with mispredict$3) same (repair$3 or restor$3)	4
☐	L1	cache same load$3 same mispredict$3 same (repair$3 or restor$3)	153

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predicted load<and>compile Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Hybrid load-value predictors**
Burtscher, M.; Zorn, B.G.;
Computers, IEEE Transactions on , Volume: 51 , Issue: 7 , July 2002
Pages:759 - 774

[Abstract] [PDF Full-Text (2294 KB)] **IEEE JNL**

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2 **Detecting global stride locality in value streams**
Huiyang Zhou; Flanagan, J.; Conte, T.M.;
Computer Architecture, 2003. Proceedings. 30th Annual International Symposium on , 9-11 June 2003
Pages:324 - 335

[Abstract] [PDF Full-Text (361 KB)] **IEEE CNF**

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3 **Silent stores and store value locality**
Lepak, K.M.; Bell, G.B.; Lipasti, M.H.;
Computers, IEEE Transactions on , Volume: 50 , Issue: 11 , Nov. 2001
Pages:1174 - 1190

[Abstract] [PDF Full-Text (4282 KB)] **IEEE JNL**

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4 **Improving value communication for thread-level speculation**
Steffan, J.G.; Colohan, C.B.; Zhai, A.; Mowry, T.C.;
High-Performance Computer Architecture, 2002. Proceedings. Eighth International Symposium on , 2-6 Feb. 2002
Pages:65 - 75

[Abstract] [PDF Full-Text (441 KB)] IEEE CNF

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5 **A high-bandwidth memory pipeline for wide issue processors**
Sangyeun Cho; Pen-Chung Yew; Gyungho Lee;
Computers, IEEE Transactions on , Volume: 50 , Issue: 7 , July 2001
Pages:709 - 723

[Abstract] [PDF Full-Text (580 KB)] IEEE JNL

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6 **A decoupled predictor-directed stream prefetching architecture**
Sair, S.; Sherwood, T.; Calder, B.;
Computers, IEEE Transactions on , Volume: 52 , Issue: 3 , March 2003
Pages:260 - 276

[Abstract] [PDF Full-Text (1356 KB)] IEEE JNL

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7 **Modeling value speculation: an optimal edge selection problem**
Chao-ying Fu; Bodine, J.T.; Conte, T.M.;
Computers, IEEE Transactions on , Volume: 52 , Issue: 3 , March 2003
Pages:277 - 292

[Abstract] [PDF Full-Text (2312 KB)] IEEE JNL

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8 **A method for design and performance modeling of client/server systems**
Menasce, D.A.; Gomaa, H.;
Software Engineering, IEEE Transactions on , Volume: 26 , Issue: 11 , Nov. 2000
Pages:1066 - 1085

[Abstract] [PDF Full-Text (520 KB)] IEEE JNL

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9 **Intelligent distributed simulation and control of power plants**
Lee, K.Y.; Perakis, M.; Sevcik, D.R.; Santoso, N.I.; Lauslerer, G.K.; Samad, T.;
Energy Conversion, IEEE Transactions on , Volume: 15 , Issue: 1 , March 2000
Pages:116 - 123

[Abstract] [PDF Full-Text (104 KB)] IEEE JNL

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10 **Hardware-based pointer data prefetcher**
Shih-Chang Lai;
Computer Design, 2003. Proceedings. 21st International Conference on , 13-15 Oct. 2003
Pages:290 - 298

[Abstract] [PDF Full-Text (305 KB)] IEEE CNF

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11 **Combining software and hardware monitoring for improved power and performance tuning**
Chi, E.; Salem, A.M.; Bahar, R.I.; Weiss, R.;
Interaction Between Compilers and Computer Architectures, 2003. INTERACT-7 2003. Proceedings. Seventh Workshop on , 8 Feb. 2003
Pages:57 - 64

[Abstract] [PDF Full-Text (271 KB)] IEEE CNF

12 **Local scheduling techniques for memory coherence in a clustered VLIW processor with a distributed data cache**
Gibert, E.; Sanchez, J.; Gonzalez, A.;
Code Generation and Optimization, 2003. CGO 2003. International Symposium on , 23-26 March 2003
Pages:193 - 203

[Abstract] [PDF Full-Text (294 KB)] IEEE CNF

13 **Adaptive grid refinement and multigrid on cluster computers**
Mitchell, W.F.;
Parallel and Distributed Processing Symposium., Proceedings 15th International , 23-27 April 2001
Pages:1211 - 1215

[Abstract] [PDF Full-Text (224 KB)] IEEE CNF

14 **Speculative precomputation: long-range prefetching of delinquent loads**
Collins, J.D.; Hong Wang; Tullsen, D.M.; Hughes, C.; Yong-Fong Lee; Lavery, D.; Shen, J.P.;
Computer Architecture, 2001. Proceedings. 28th Annual International Symposium on , 30 June-4 July 2001
Pages:14 - 25

[Abstract] [PDF Full-Text (232 KB)] IEEE CNF

15 **Measuring experimental error in microprocessor simulation**
Desikan, R.; Burger, D.; Keckler, S.W.;
Computer Architecture, 2001. Proceedings. 28th Annual International Symposium on , 30 June-4 July 2001
Pages:266 - 277

[Abstract] [PDF Full-Text (152 KB)] IEEE CNF

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predicted load<and>compile Search

☐ Check to search within this result set

Results Key:
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16 **Static identification of delinquent loads**
Panait, V.-M.; Sasturkar, A.; Weng-Fai Wong;
Code Generation and Optimization, 2004. CGO 2004. International Symposium on , 20-24 March 2004
Pages:303 - 314

[Abstract] [PDF Full-Text (441 KB)] **IEEE CNF**

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17 **Compiler optimization of memory-resident value communication between speculative threads**
Antonia Zhai; Colohan, C.B.; Steffan, J.G.;
Code Generation and Optimization, 2004. CGO 2004. International Symposium on , 20-24 March 2004
Pages:39 - 50

[Abstract] [PDF Full-Text (384 KB)] **IEEE CNF**

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18 **Quantifying instruction criticality**
Tune, E.S.; Tullsen, D.M.; Calder, B.;
Parallel Architectures and Compilation Techniques, 2002. Proceedings. 2002 International Conference on , 22-25 Sept. 2002
Pages:104 - 113

[Abstract] [PDF Full-Text (379 KB)] **IEEE CNF**

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19 **Loose loops sink chips**
Borch, E.; Tune, E.; Manne, S.; Emer, J.;

High-Performance Computer Architecture, 2002. Proceedings. Eighth International Symposium on , 2-6 Feb. 2002
Pages:299 - 310

[Abstract] [PDF Full-Text (384 KB)] IEEE CNF

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20 **Exploring last n value prediction**
Burtscher, M.; Zorn, B.G.;
Parallel Architectures and Compilation Techniques, 1999. Proceedings. 1999 International Conference on , 12-16 Oct. 1999
Pages:66 - 76

[Abstract] [PDF Full-Text (120 KB)] IEEE CNF

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		DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ	
☐	L13	l11 and (repair$3 or restor$3)	0
☐	L12	L11 and cache miss	1
☐	L11	predicted load	105
☐	L10	mispredict$4 with load	4
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
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